Logic family

In computer engineering, a **logic family** may refer to one of two related concepts. A logic family of monolithic digital integrated circuit devices is a group of electronic logic gates constructed using one of several different designs, usually with compatible logic levels and power supply characteristics within a family. Many logic families were produced as individual components, each containing one or a few related basic logical functions, which could be used as "building-blocks" to create systems or as so-called "glue" to interconnect more complex integrated circuits. A "logic family" may also refer to a set of techniques used to implement logic within VLSI integrated circuits such as central processors, memories, or other complex functions. Some such logic families use static techniques to minimize design complexity. Other such logic families, such as domino logic, use clocked dynamic techniques to minimize size, power consumption and delay.

Before the widespread use of integrated circuits, various solid-state and vacuum-tube logic systems were used but these were never as standardized and interoperable as the integrated-circuit devices. The most common logic family in modern semiconductor devices is metal–oxide–semiconductor (MOS) logic, due to low power consumption, small transistor sizes, and high transistor density.

Transistor-Transistor Logic (TTL)

Introduction to Logic Families:

Logic Gates like NAND, NOR are used in daily applications for performing logic operations. The Gates are manufactured using semiconductor devices like BJT, Diodes or FETs. Different Gate's are constructed using Integrated circuits. Digital logic circuits are manufactured depending on the specific circuit technology or logic families.

The different logic families are:

1. RTL(Resistor Transistor Logic)
2. DTL(Diode Transistor Logic)
3. TTL(Transistor Transistor Logic)
4. ECL(Emitter Coupled Logic)
5. CMOS(Complementary Metal Oxide Semiconductor Logic)

Out of these RTL and DTL are rarely used.

Features of Logic Families:

1. Fan Out: Number of loads the output of a GATE can drive without effecting its usual performance. By load we mean the amount of current required by the input of another Gate connected to the output of the given gate.
2. Power Dissipation**:** It represents the amount of power needed by the device. It is measured in mW. It is usually the product of supply voltage and the amount of average current drawn when the output is high or low.
3. Propagation Delay: It represents the transition time which elapses when the input level changes. The delay which occurs for the output to make its transition is the propagation delay.
4. Noise Margin: It represents the amount of noise voltage allowed at the input, which doesn't effects the standard output.

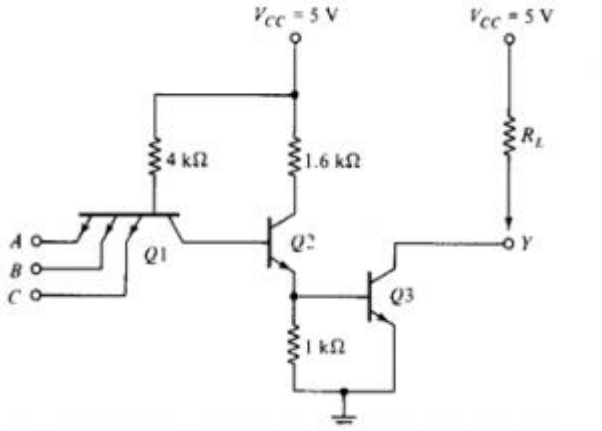
Introduction to TTLs:

It is a logic family consisting completely of transistors. It employs transistor with multiple emitters. Commercially it starts with the 74 series like the 7404, 74S86 etc. It was build in 1961 by James L Bui and commercially used in logic design in 1963

Classification of TTL:

TTLs are classified based on the output.

1. Open Collector Output: The main feature is that its output is 0 when low and floating when high. Usually an external Vcc may be applied.

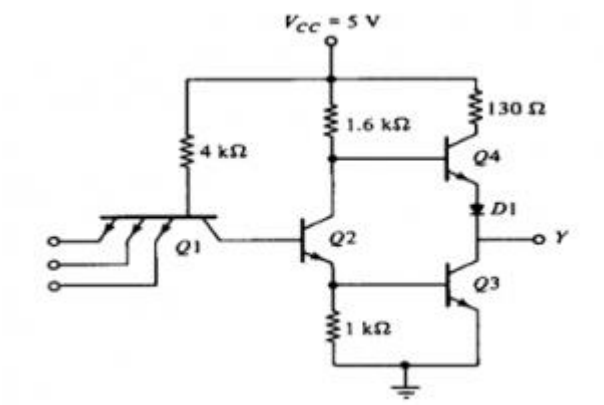


Transistor Q1 actually behaves as cluster of diodes placed back to back. With any of the input at logic low, corresponding emitter base junction is forward biased and the voltage drop across the base of Q1 is around 0.9V, not enough for the transistors Q2 and Q3 to conduct. Thus output is either floating or Vcc, i.e. High level.

Similarly when all inputs are high, all base emitter junctions of Q1 are reverse biased and transistor Q2 and Q3 get enough base current and are in saturation mode. Clearly output is at logic low. (For a transistor to go to saturation, collector current should be greater than β times the base current).

2. Totem Pole Output:

Totem Pole means addition of an active pull up circuit in the output of the Gate which results in reduction of propagation delay.



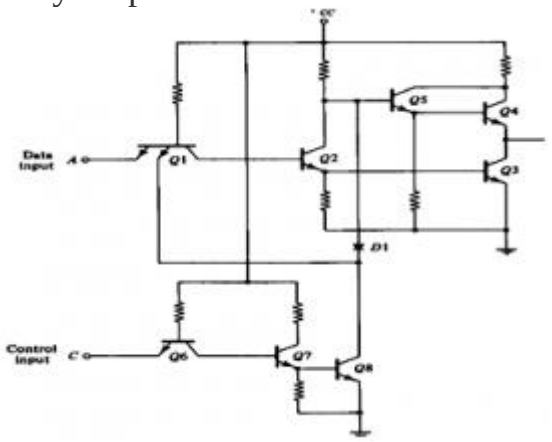
Logic operation is same as the open collector output. Use of transistors Q4 and diode is to provide quick charging and discharging of parasitic capacitance across Q3. Resistor is used to keep the output current to a safe value.

3. Three state Gate:

It provides 3 state output.

1. Low level state when lower transistor is ON and upper transistor is OFF.
2. High level state when lower transistor is OFF and upper transistor is ON.

3. Third state when both transistors are OFF. It allows a direct wire connection of many outputs.



Features of TTL Family:

1. Logic low level is at 0 or 0.2V.
2. Logic high level is at 5V.
3. Typical fan out of 10. It means it can support at most 10 gates at its output.
4. A basic TTL device draws a power of almost 10mW, which reduces with use of schottky devices.
5. Average propagation delay is about 9ns.
6. The noise margin is about 0.4V.

Series of TTL IC:

TTL ICs mostly start with the 7 series. It has basically 6 subfamilies given as:

1. Low Power device with propagation delay of 35 ns and power dissipation of 1mW.
2. Low power Schottky device with delay of 9ns
3. Advanced Schottky device with delay of 1.5ns.
4. Advanced low power Schottky device with delay of 4 ns and power dissipation of 1mW.

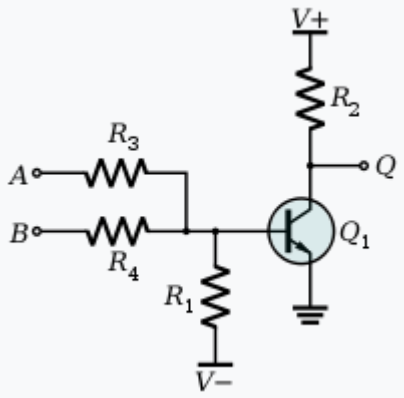
Resistor–transistor logic

Resistor–transistor logic (**RTL**) (sometimes also **transistor–resistor logic** (**TRL**)) is a class of digital circuits built using resistors as the input network and bipolar junction transistors (BJTs) as switching devices. RTL is the earliest class of transistorized digital logic circuit used; other classes include diode–transistor logic (DTL) and transistor–transistor logic (TTL). RTL circuits were first constructed with discrete components, but in 1961 it became the first digital logic family to be produced as

a monolithic integrated circuit. RTL integrated circuits were used in the Apollo Guidance Computer, whose design was begun in 1961 and which first flew in 1966

RTL inverter:-

A bipolar transistor switch is the simplest RTL gate (inverter or NOT gate) implementing logical negation.[2] It consists of a common-emitter stage with a base resistor connected between the base and the input voltage source. The role of the base resistor is to expand the very small transistor input voltage range (about 0.7 V) to the logical "1" level (about 3.5 V) by converting the input voltage into current. Its resistance is settled by a compromise: it is chosen low enough to saturate the transistor and high enough to obtain high input resistance. The role of the collector resistor is to convert the collector current into voltage; its resistance is chosen high enough to saturate the transistor and low enough to obtain low output resistance (high fan-out).

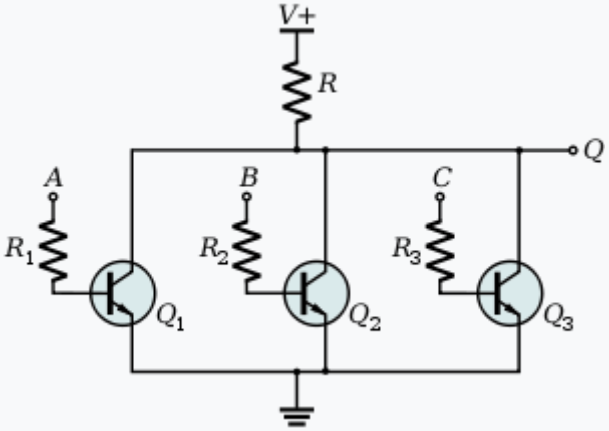


Schematic of a one-transistor RTL NOR gate.

One-transistor RTL NOR gate

With two or more base resistors (R_3 and R_4) instead of one, the inverter becomes a two-input RTL NOR gate (see the figure on the right). The logical operation OR is performed by applying consecutively the two arithmetic operations addition and comparison (the input resistor network acts as a parallel *voltage summer* with equally weighted inputs and the following common-emitter transistor stage as a *voltage comparator* with a threshold about 0.7 V). The equivalent resistance of all the resistors connected to logical "1" and the equivalent resistance of all the resistors connected to logical "0" form the two legs of a composed voltage divider driving the transistor. The base resistances and the number of the inputs are chosen (limited) so that only one logical "1" is sufficient to create base-emitter voltage exceeding the threshold and, as a result, saturating the transistor. If all the input voltages are low (logical

"0"), the transistor is cut-off. The pull-down resistor R_1 biases the transistor to the appropriate on-off threshold. The output is inverted since the collector-emitter voltage of transistor Q_1 is taken as output, and is high when the inputs are low. Thus, the analog resistive network and the analog transistor stage perform the logic function NOR.



Schematic of a multi-transistor RTL NOR gate used to build the Apollo Guidance Computer

Photograph of the dual NOR gate chip used to build the Apollo Guidance Computer

Flatpack RTL NOR gate integrated circuits in the Apollo guidance computer

Multi-transistor RTL NOR gate[edit]

The limitations of the one-transistor RTL NOR gate are overcome by the multi-transistor RTL implementation. It consists of a set of parallel-connected transistor switches driven by the logic inputs (see the figure on the right). In this configuration, the inputs are completely separated and the number of inputs is limited only by the small leakage current of the cut-off transistors at output logical "1". The same idea was used later for building DCTL, ECL, some TTL (7450, 7460), NMOS and CMOS gates.

Advantages[edit]

The primary advantage of RTL technology was that it used a minimum number of transistors. In circuits using discrete components, before integrated circuits, transistors were the most expensive component to produce. Early IC logic production (such as Fairchild's in 1961) used the

same approach briefly, but quickly transitioned to higher-performance circuits such as diode–transistor logic and then transistor–transistor logic (starting 1963 at Sylvania), since diodes and transistors were no more expensive than resistors in the IC.

Limitations[edit]

The disadvantage of RTL is its high power dissipation when the transistor is switched on, by current flowing in the collector and base resistors. This requires that more current be supplied to and heat be removed from RTL circuits. In contrast, TTL circuits with "totem-pole" output stage minimize both of these requirements.

Another limitation of RTL is its limited fan-in: 3 inputs being the limit for many circuit designs, before it completely loses usable noise immunity. It has a low noise margin. Lancaster says that integrated circuit RTL NOR gates (which have one transistor per input) may be constructed with "any reasonable number" of logic inputs, and gives an example of an 8-input NOR gate.[1] A standard integrated circuit RTL NOR gate can drive up to 3 other similar gates. Alternatively, it has enough output to drive up to 2 standard integrated circuit RTL "buffers", each of which can drive up to 25 other standard RTL NOR gates.

CMOS

Complementary metal–oxide–semiconductor (**CMOS**), also known as **complementary-symmetry metal–oxide–semiconductor** (**COS-MOS**), is a type of MOSFET (metal–oxide–semiconductor field-effect transistor) fabrication process that uses complementary and symmetrical pairs of p-type and n-type MOSFETs for logic functions.[1] CMOS technology is used for constructing integrated circuit (IC) chips, including microprocessors, microcontrollers, memory chips (including CMOS BIOS), and other digital logic circuits. CMOS technology is also used for analog circuits such as image sensors (CMOS sensors), data converters, RF circuits (RF CMOS), and highly integrated transceivers for many types of communication.

Mohamed M. Atalla and Dawon Kahng invented the MOSFET at Bell Labs in 1959, and then demonstrated the PMOS (p-type MOS) and NMOS (n-type MOS) fabrication processes in 1960. These processes were later combined and adapted into the complementary MOS (CMOS) process by Chih-Tang Sah and Frank Wanlass at Fairchild Semiconductor in 1963. RCA commercialized the technology with the trademark "COS-MOS" in the late 1960s, forcing other manufacturers to find another name, leading to "CMOS" becoming

the standard name for the technology by the early 1970s. CMOS eventually overtook NMOS as the dominant MOSFET fabrication process for very large-scale integration (VLSI) chips in the 1980s, and has since remained the standard fabrication process for MOSFET semiconductor devices in VLSI chips. As of 2011, 99% of IC chips, including most digital, analog and mixed-signal ICs, are fabricated using CMOS technology.

Two important characteristics of CMOS devices are high noise immunity and low static power consumption.[3] Since one transistor of the MOSFET pair is always off, the series combination draws significant power only momentarily during switching between on and off states. Consequently, CMOS devices do not produce as much waste heat as other forms of logic, like NMOS logic or transistor–transistor logic (TTL), which normally have some standing current even when not changing state. These characteristics allow CMOS to integrate a high density of logic functions on a chip. It was primarily for this reason that CMOS became the most widely used technology to be implemented in VLSI chips.

The phrase "metal–oxide–semiconductor" is a reference to the physical structure of MOS field-effect transistors, having a metal gate electrode placed on top of an oxide insulator, which in turn is on top of a semiconductor material. Aluminium was once used but now the material is polysilicon. Other metal gates have made a comeback with the advent of high-κ dielectric materials in the CMOS process, as announced by IBM and Intel for the 45 nanometer node and smaller sizes.